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[54] **METHOD AND SYSTEM FOR DYNAMICALLY RECONFIGURING A REGISTER FILE IN A VECTOR PROCESSOR**

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[58] **Field of Search** 395/800, 411

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[57] **ABSTRACT**

A controller is coupled to a plurality of registers arranged in an array having a physical configuration of N rows of registers and M columns of registers. A size register within the controller is provided for receiving a selected vector size parameter, which specifies a number of registers comprising a vector register. In response to the vector size parameter, columns in the register array are selected and concatenated to form a vector register having at least a number of registers equal to the vector size parameter. An offset parameter may be utilized to select columns that form a vector register from the M number of columns in the array. Multiple arithmetic logic units, where one arithmetic logic unit is coupled to each row of registers are utilized to perform vector operations. Any register in the array may be utilized to store a vector element or a scalar expression. Vector register lengths, and the number of vector registers, may be dynamically configured by setting the vector size parameter and the offset parameter in the controller.

7 Claims, 8 Drawing Sheets